NQ verification 2023–24 round 2

Qualification verification summary report

Section 1: verification group information

Verification group name:	**Practical Electronics**
Verification activity:	**Visit**
Date published:	**July 2024**

National Course verified

Unit code	Unit level	Unit title
C860 75	National 5	Practical Electronics

Section 2: comments on assessment

Assessment approaches

There was a range of practical activity tasks available for centres to select from and all were similar in complexity. Regardless of the task chosen, or the experience of the assessor and internal verifier, many candidates had similar strengths and weakness. Many candidates found the following skills challenging: creating complete and accurate circuit layout diagrams; adding appropriate test points; writing up test plans; maintaining an up-to-date and complete logbook with evidence of testing and evaluation; carrying out testing on each subsystem and the whole solution; and missing out a wiring schedule. Most candidates did reasonably well on constructing each subsystem and completing a circuit simulation that meets the brief.

All aspects of each available task provided sufficient opportunity for candidates to demonstrate different levels of performance, from analysis and design through to building, testing and final reporting.

The marking instructions, supported by Understanding Standards support materials, allowed assessors and internal verifiers to award appropriate credit to key levels of performance in all key areas. The key areas include design, construction, testing and reporting on the candidate's solution. The marking instructions also allowed assessors and internal verifiers to differentiate between different levels of performance in all key areas of the practical activity.

Points to note regarding assessment approaches

Price of components:

- The bill of materials should include an 'item ID' (such as R1, R2, LED 1, IC1, TR1, BZ1).
- The item ID should be carried through Yenka simulation, breadboard planning, stripboard (layout) planning and testing.
- For a detailed list of components, there should be a table with a list of components, serial code, number of components, supplier, unit price and total price. To work out the total price of each type of component, candidates should investigate the price for a batch of components rather than multiplying the unit price by the number of components.

Simulated solution:

- Yenka simulation should be clearly sectioned off and labelled with input, process and output.
- The assessor should check that the candidate's simulation meets the brief of that assignment.
- If a candidate struggles to complete a simulated solution, the assessor should provide an accurate and completed simulated solution, so that the candidate can confidently attempt the rest of the assignment.
- Logic points can be added on the simulated solution, which are useful for testing the solution.

Layout diagram:

- Candidates struggling with 'Detailed component layout diagrams' should be provided with the assessor's completed solution. This would allow candidates to achieve full marks on the constructing stages of the practical activity. The assessor should encourage candidates to colour code and number each wire on the process subsystem layout diagram. This is to help candidates during circuit construction, circuit testing and circuit repair.
- If the assessor is providing a solution to the candidate, make sure the breaks and components are in the correct place so that the candidate can confidently assemble a working solution to the problem. The assessor should also check that their own work is accurate and complete with physical symbolds and not circuit symbols.
- If any candidate wishes to use their own stripboard layout, then make sure the candidate's layout is complete and electrically reliable for the next stage.
- Candidates are also encouraged to add test points on their layout diagram.
- Candidates may solder horizontal screw terminal blocks on each subsystem, rather than single level terminal blocks between each subsystem. If this is the case, the candidates should include the soldered horizontal screw terminal blocks on the layout diagram, labelled with an appropriate test point number for each screw.
- The stripboard plans and physical circuit should match exactly.
- Candidates should use wiring conventions. Red wire should only be used for power connections, both on the individual boards and in the loom. Black wire should only be used for ground connections. Any other colour of wire can be used for signals. There should be different colours for different signals: if all the wires on the subsystem have the same colour, then this suggests that each point on the subsystem has the same signal or potential. If red and black are not available, document using two other colours. In this case, the two chosen colours cannot be used for any signal wiring.

Construction and neatness of each subsystem:

- For circuit construction, it is good practice not to solder an integrated circuit (IC) onto a stripboard as it may damage the components inside it. A dual-in-line holder should be soldered on first.
- Candidates should follow the correct wiring convention for the construction of each subsystem and circuit solution. Again, this should help candidates to identify faults during testing and repair.
- The assessor should regularly check each constructed subsystem and provide constructive feedback to the candidate. This includes connecting the correct pins for each IC to the power rails.
- Make sure candidates follow the stripboard layout exactly with the correct breaks for ICs and elsewhere in each subsystem.
- Make sure the wires and components are flushed.

Labelling:

- Avoid sticking a label on an IC chip.
- Make sure the label for a switch includes its function, for example 'SPDT 1 – master switch'.

Wiring and assembly:

- Leads between circuit boards should be protected by sleeving or some other form of protection.
- Make sure candidates have produced an accurate wiring schedule.
- Input, process and output boards should be easily disconnected from each other using either crimp connectors or terminal blocks in the wiring looms. Avoid using heat shrink, unless a component needs to be added to a subsystem but cannot be soldered directly onto it.
- For secureness, make sure the input/output lead is hooked and soldered.

Test points:

- Make sure candidates are aware that test points at each end of the subsystem can be used for continuity testing. This is especially useful for gaining an extra mark for electrical reliability in the wiring and assembly section.

Test plan:

- For test planning, candidates are encouraged to present three different test plans: pre-testing each subsystem; power testing each subsystem; and power testing the three subsystems connected together.
- Power testing should also include: results for each test point; using logic probes and recording a logic level for relevant pins of an IC (under certain light conditions and switching positions); and electrical continuity between subsystems.
- Candidates should produce a table of each type of test plan. The test plan of the whole solution should include a comparison of results from the simulated solution and the candidate's results from their own constructed solution.

Testing and repair:

- Encourage candidates to modify the assessor's stripboard layout, for example, TP1 for the 0 V rail line, for testing and subsequent repair.
- If there were changes to the circuit during testing and repair, make sure candidates have evidenced this in their simulation, stripboard layout (either their own or the assessor's), price of components and logbook.

Evaluation:

- Make sure the evaluation is robust enough to include problems encountered, how they were resolved and the next steps.

Assessment judgements

Overall, the practical activity met the standard as most deviations were within tolerance. Most deviations were due to the experience of the assessor in delivering the course and applying the marking scheme. However, the marking scheme is robust enough to ensure that deviations in marks given were within tolerance.

The marking instructions and subsequent instructions to candidates functioned as expected, with all centres' marks being within tolerance. Where a centre had an 'accepted with recommendations', this was usually due to inexperience with the industrial aspects of electronics, such as clarity of layout diagrams and conventions used (such as colour coding of layout wires), soldering and interconnection techniques for circuit boards, test planning and resulting. If candidates struggle to produce a stripboard layout, the assessor should provide a fully annotated solution to use for circuit construction. Similarly, if a candidate struggles to complete a simulated solution, the assessor should provide an accurate and completed simulated solution, so that the candidate can confidently attempt the rest of the assignment.

Centres should also ensure that they have a range of suitable tools, consumables and other resources in order that candidates can maximise marks for the practical aspects of the course.

Layout diagrams should include all interconnections and track cuts. They should be created using the actual footprint of each component and not the simulation circuit symbol.

The actual circuits built should replicate the layout diagrams to ensure consistency, but it may be necessary to make changes; for example, axial capacitors may become radial capacitors due to component ordering.

Professional circuit labelling kits can be purchased so that candidates will not need to use a marker pen to label stripboards. The colour of wiring used should reflect industrial practice and not just what is available.

During circuit construction, the assessor should check each board for accuracy with suitable feedback, so that candidates can confidently amend it and proceed to the next stage.

Another major feature of assessment judgement is internal verification. The internal verifier should also be aware of the standards expected, and there should be notes on agreements

and disagreements to justify the marks awarded on each part of the sampled candidate's work.

Points to note regarding assessment judgements

Layout diagram:

- There was leniency when assessing 'Detailed component layout diagrams'. For some candidates, there were either no track breaks or breaks were in the wrong place.
- Test points should be planned and included in the layout diagram.
- The assessor should note how much help was provided for the candidate and mark their work accordingly.

Construction and neatness of subsystem layout:

- All the candidates sampled did not follow the correct convention for wiring. All of them used green wires in the process subsystem constructed; one candidate also used white wires. For 'Neatness of subsystem layout', candidates should also be assessed on the correct convention of colour codes. For example, pin 14 should be connected to the +Vs rail with a red wire; pin 7 should be connected to the 0 V rail with a black wire.

Labelling:

- There was leniency in marking labelling subsystems. Some candidates were awarded full marks even though they missed out labelling a switch with its function, or LEDs, LDRs or 555 timer.

Wiring and assembly:

- Candidates should use a method of identifying wires and connectors by numbering or colour coding. A wiring schedule must be provided to gain at least one mark.
- The schedule should include the colour and number of each wire, its connections and its function. For the wiring to be complete, all the input/output wires must be present in each subsystem, which is presented in the stripboard layout.
- Some candidates were penalised for neatness in the wrong section.
- Check for electrical reliability for any candidate who has scored three marks for wiring and assembly. Continuity testing is used in the testing and repair stage: if the candidate did not include this in the report, then the assessor and internal verifier should check for continuity; otherwise, the candidate would be disadvantaged in achieving full marks for wiring and assembly.

Independence and safety:

- For constructing each subsystem, centre staff did not provide comments to justify marks awarded for safety and independence for certain candidates.

Test points:

- Test points should be planned and included in the layout diagram.
- Make sure there are test points for the input and output ends of each subsystem.
- If screw terminal blocks are soldered on each subsystem, make sure that each screw is labelled with the correct test point on the layout diagram.

Testing:

- For good practice, pre-power up should be put in a table instead of written paragraphs.

The majority of the candidates sampled had difficulty with similar areas, such as system or block diagram, application of test pins and the subsequent circuit testing.

Attention was drawn to the appropriate area of the marking scheme. Detailed feedback was given on the application of the marking descriptors to the candidate's circuitry.

Section 3: general comments

Over the last few sessions, there were more experienced staff delivering the course. In addition, there were more opportunities for staff to share experiences through social media as well as regional networking. This has improved the internal verification process as well as overall performance.

The course had a good balance of practical hands-on elements, as well as more demanding tasks such as circuit layout diagrams, testing and evaluation.

As expected, the more experienced assessors were able to help candidates perform better. However, there is a wealth of support available to all assessors to tap into if they wish. There is also a strong support network for assessors and internal verifiers using social media.