Next Generation Higher National Unit Specification

Digital Electronics: Digital System Design (SCQF level 8)

Unit code: J7C3 48

SCQF level: 8 (24 SCQF credit points)

Valid from: session 2023–24

Prototype unit specification for use in pilot delivery only (version 1.0) October 2023

This unit specification provides detailed information about the unit to ensure consistent and transparent assessment year on year.

This unit specification is for teachers and lecturers and contains all the mandatory information required to deliver and assess the unit.

This edition: October 2023 (version 1.0)

Unit purpose

This unit gives learners the knowledge of digital electronics they need to design, build and test state machines that interface with real-world signals, and implement these on programmable logic devices. The unit covers:

- characteristics and use of analogue to digital converters (ADCs)
- characteristics and use of digital to analogue converters (DACs)
- design and use of finite state machines (FSMs)
- programmable logic devices (PLDs) and hardware description language (HDL)

Learners have the opportunity to develop their self-management and creative problem-solving skills as they identify solutions to real-world problems.

The unit is aimed at learners who want to develop their digital electronics design and analysis skills, to support an industrial career in electronics or instrumentation and control engineering.

It is also aimed at learners who want to develop the practical, personal and professional skills required for a successful career as an engineering technician.

Entry to the unit is at your centre's discretion. However, we recommend that learners have one or more of the following:

- broad knowledge and understanding of digital electronics at SCQF level 7, for example a pass at SCQF level 7 in a subject related to electronics principles
- relevant SCQF level 7 qualifications, for example Advanced Higher Physics or Engineering Science, or a Higher National Certificate (HNC) in a related engineering subject
- relevant, equivalent work experience

Unit outcomes

Learners who complete this unit can:

1 design, simulate, build, test and evaluate analogue to digital converter (ADC) and digital to analogue converter (DAC) conversion circuits
2 design, simulate, build, test and evaluate sequential finite state machines (FSMs)
3 design, simulate, build, test and evaluate programmable logic device (PLD) circuits using a hardware description language (HDL)

Evidence requirements

You assess the unit holistically, using a portfolio of evidence generated by learners. Learners must produce a reflective report for each outcome, evaluating the knowledge and skills they have gained. They should produce reports to a professional standard, using word-processing software.

Evidence should principally be made up of written and/or oral recorded evidence, typically design documents, circuit diagrams, netlists, screenshots, photographs or videos, artefacts (hardware), code, or critical evaluation. Learners must generate evidence under unsupervised, open-book conditions.

You can find more information in the ‘Additional guidance’ section.

To successfully achieve the unit, learners must provide evidence for the following outcomes:

Outcome 1

1a Critically compare two ADCs from the following list, in terms of their operation, and their static and dynamic parameters:

- dual slope ADC
- flash ADC
- successive approximation ADC
- delta-sigma ADC

Learners should compare two different ADCs each time the outcome is assessed.

1b Critically compare binary weighted DACs with R-2R ladder DACs in terms of their operation, and their static and dynamic parameters.

1c Using an ADC and a DAC, design a circuit to convert an analogue signal to a digital signal, and then back again to analogue. Simulate this circuit to prove its functionality.

1d Build the circuit designed in 1c on breadboard, stripboard, printed circuit board or equivalent.

1e Test the circuit built in 1d using hardware test and debugging tools, and evaluate the test results against a pre-defined specification that includes static and dynamic parameters.

1f Using an example, describe how aliasing and the Nyquist theory determine the ADC sampling rate.

Outcome 2

2a Using examples, critically compare the operation of Mealy and Moore sequential FSMs.

2b Using state and timing diagrams, and transition and excitation tables, design a Mealy or Moore sequential FSM that has at least one input, one output, three stable states and two unused states. The design must use either JK or D-type bistables and must include evidence of:

- minimisation of combinational logic required
- avoidance of non-determinism
- inclusion of a stuttering transition
- avoidance of static hazards
- avoidance of dynamic hazards

2c Simulate the circuit designed in 2b to prove its functionality.

2d Build the circuit designed in 2b on breadboard, stripboard, printed circuit board or equivalent.

2e Test the circuit built in 2d using hardware test and debugging tools, and evaluate the test results against a pre-defined specification that includes static and dynamic parameters.

2f Describe how sequential FSMs can be optimised for speed, architecture, standardisation and space, clearly explaining what each of these terms mean.

Outcome 3

3a Critically compare two PLDs from the following list, in terms of their structure, characteristics and operation:

- programmable logic array (PLA)
- programmable array logic (PAL)
- field programmable gate array (FPGA)
- application-specific integrated circuit (ASIC)

Learners should compare two different PLDs each time the outcome is assessed.

3b Using an HDL and an integrated development environment (IDE), design a Mealy or Moore sequential FSM that has at least one input, one output, three stable states and two unused states. The HDL code should include:

- one or more libraries
- one or more entity declarations
- one or more architecture declarations
- a structural model

3c In the IDE, write a testbench to simulate the circuit designed in 3b and use this to fully evaluate the circuit's functionality.

3d With consideration of a specific hardware device, synthesise the design in 3b, optimising for one of the following:

- latency
- architecture
- space
- power
- speed

Learners should work with a different optimisation parameter each time the outcome is assessed.

3e Critically evaluate the IDE used in terms of its editing, analysis, testing, debugging and synthesis capabilities.

Knowledge and skills

The following table shows the knowledge and skills covered by the unit outcomes:

Knowledge	Skills
Outcome 1 Learners should understand: ♦ the operation of dual slope, flash, successive approximation and delta-sigma ADCs ♦ the static characteristics of dual slope, flash, successive approximation and delta-sigma ADCs ♦ the dynamic characteristics of dual slope, flash, successive approximation and delta-sigma ADCs ♦ the operation of binary weighted and R-2R DACs ♦ the static characteristics of binary weighted and R-2R DACs ♦ the dynamic characteristics of binary weighted and R-2R DACs	**Outcome 1** Learners can: ♦ design an ADC circuit ♦ design a DAC circuit ♦ simulate an ADC circuit to prove functionality ♦ simulate a DAC circuit to prove functionality ♦ build a hardware ADC circuit ♦ build a hardware DAC circuit ♦ use hardware test and debugging tools to prove an ADC circuit meets static and dynamic specifications ♦ use hardware test and debugging tools to prove a DAC circuit meets static and dynamic specifications
Outcome 2 Learners should understand: ♦ the operation of Mealy sequential FSMs ♦ the operation of Moore sequential FSMs ♦ the design parameters affecting sequential FSMs, including minimisation of combinational logic, avoidance of non-determinism, stuttering transitions, and avoidance of static and dynamic hazards ♦ how sequential FSMs can be optimised for speed, architecture, standardisation and space	**Outcome 2** Learners can: ♦ use state and timing diagrams, and transition and excitation tables to design a sequential FSM ♦ simulate a sequential FSM to prove functionality ♦ build a hardware sequential FSM ♦ use hardware test and debugging tools to prove a sequential FSM meets specifications

Knowledge	Skills
Outcome 3 Learners should understand: ♦ the structure, characteristics and operation of PLAs, PALs, FPGAs and ASICs ♦ the editing, analysis, testing, debugging and synthesis capabilities of an IDE ♦ the use of libraries, entities, architectures and structural declarations in HDL ♦ how HDL synthesis can optimise for latency, architecture, space, power and/or speed	**Outcome 3** Learners can: ♦ use an HDL and an IDE to design a sequential FSM ♦ design and use an HDL testbench to prove functionality of an HDL design ♦ synthesise an HDL design for a specific device, using optimisation

Meta-skills

Throughout the unit, learners develop meta-skills to enhance their employability in the engineering sector.

Self-management

Learners develop the meta-skill of initiative as they fault-find and solve problems with their designs.

Social intelligence

Learners develop the meta-skills of communicating and collaborating as they work with others on formative activities.

Innovation

Learners develop their creativity when they come up with designs that are optimised to meet specified requirements.

Literacies

Numeracy

Learners develop numeracy skills by performing engineering calculations when evaluating devices and circuits.

Communication

Learners develop communication skills by studying the course materials and engaging with you and their peers.

Digital

Learners develop digital skills and computer literacy by using engineering simulation software, and by writing programs and using an IDE.

Delivery of unit

This unit is part of the Higher National Diploma (HND) in Engineering. The framework includes mandatory and optional units, and you can tailor the selected combination of units to specific engineering pathway needs.

This unit complements, and can be delivered alongside, Analogue Electronics: Design and Analysis.

While the exact time allocated to the unit is at your centre's discretion, the notional design length is 120 hours.

The amount of time you allocate to each outcome is also at your discretion. We suggest the following distribution of time, including assessment:

Outcome 1 — Design, simulate, build, test and evaluate analogue to digital converter (ADC) and digital to analogue converter (DAC) conversion circuits
(40 hours)

Outcome 2 — Design, simulate, build, test and evaluate sequential finite state machines (FSMs)
(40 hours)

Outcome 3 — Design, simulate, build, test and evaluate programmable logic device (PLD) circuits using a hardware description language (HDL)
(40 hours)

Additional guidance

The guidance in this section is not mandatory.

Content and context for this unit

This unit provides learners with knowledge of conversion devices and state machines, so they can design and analyse digital control systems typical of those found in electronics, and control and instrumentation engineering.

Design, simulate, build, test and evaluate analogue to digital converter (ADC) and digital to analogue converter (DAC) conversion circuits (outcome 1)

In this outcome, learners study ADCs and DACs. They design a combined circuit from initial specification to evaluation of results.

You could start by introducing concepts of sampling, Nyquist theory and aliasing. For ADCs, you should teach learners about generic characteristics such as reference voltage, resolution, full scale input, conversion rate, and the difference between unipolar and bipolar operation. You should then cover the operation of a variety of contemporary ADCs, including dual slope, flash, successive approximation and delta-sigma ADCs. For DACs, you should cover the operation of contemporary types, including binary weighted and R-2R. You could use block diagrams to illustrate the operation of all these devices. Learners should compare the pros and cons of the different types. They should learn about:

- static parameters: accuracy and total unadjusted error, offset error and drift, differential and integral non-linearity
- dynamic parameters: total harmonic distortion, signal to noise ratio, signal to noise and distortion, and spurious free dynamic range

Encourage learners to read real datasheets and do conversion calculations. You should use case studies and industrial examples to give context to the circuits.

Design, simulate, build, test and evaluate sequential finite state machines (FSMs) (outcome 2)

In this outcome, learners study sequential FSMs. They design one of these from initial specification to evaluation of test results.

Learners should be familiar with designs using D-type bistables and JK bistables, and it is advisable to revise the operation of these devices before moving onto sequential FSMs. You should teach both Mealy and Moore FSMs and give learners the opportunity to design both; however, only one type is required for each summative assessment attempt. You should use case studies and industrial examples to give context to the circuits. Encourage learners to consult data sheets to inform their designs and use appropriate software to draw their state and timing diagrams.

Design, simulate, build, test and evaluate programmable logic device (PLD) circuits using a hardware description language (HDL) (outcome 3)

In this outcome, learners study programmable devices and HDL. They go on to design a sequential FSM for a programmable device, from initial specification to test evaluation.

Learners should understand the concept of abstraction and the differences between register transfer logic (RTL), behavioural, and structural HDL architectures. They should be able to code using mixed architecture styles. Learners should code testbenches concurrently, moving from simple functional, static tests on combinational logic, to testing timing parameters of sequential circuits, then sequential FSMs. Make sure learners follow good coding practices, including version control and using comments.

You should teach learners how to use debugging tools within the IDE; for example, breakpoints, timing diagrams, and compilation, synthesis and netlist reports. For this outcome, learners do not need to demonstrate hardware, but you should introduce them to contemporary devices. They should understand the problems encountered in optimising for hardware and transferring a working simulation to a real device.

Approaches to delivery

We recommend that you teach outcome 1 first, but this is not essential. We recommend you teach outcome 2 before outcome 3, as you can use the same specification for both summative designs.

In outcome 3, we suggest that you teach device architectures first, before moving onto HDL and the use of IDEs. It is not necessary to teach HDL or IDE use in depth; instead, use pre-written examples. The IDE used does not need to be an industrial version — a scaled-down simpler IDE is acceptable, provided it has all the features required to write, compile, test, debug and synthesise HDL, with optimisation options.

Approaches to assessment

Design, simulate, build, test and evaluate analogue to digital converter (ADC) and digital to analogue converter (DAC) conversion circuits (outcome 1)

You should encourage learners to work together during formative assessment to solve problems.

The ADC and DAC circuits learners use for summative simulation can be the same circuits they use for summative hardware build and test. Simulation should prove functional performance, and learners' circuits should be fully functional at both simulation and hardware test stages to pass the outcome. Learners can use partially pre-built circuits for hardware to save time. Learners should use contemporary debugging and hardware tools, including logic analysers. It is not necessary to test against all the static and dynamic parameters, and you should write specifications in accordance with the test equipment available. For example, if synthesised signal generators and spectrum analysers are not available, it is probably not possible to test distortion.

Learners can produce a single report covering all the outcome's knowledge and skills requirements, and including critical self-reflection, as evidence. They should accompany this with demonstrations (these could be videos, screenshots or live) of working simulations and hardware.

Design, simulate, build, test and evaluate sequential finite state machines (FSMs) (outcome 2)

You should encourage learners to work together during formative assessment to fault-find and solve problems. You could artificially introduce circuit errors to prompt this.

Learners should include logic minimisation and at least one other optimised characteristic in their design for summative assessment. It should also demonstrate avoidance of non-determinism and hazards, and include a stuttering transition. Simulation should prove functional performance, and learners' circuits should be fully functional (without hazards) at both simulation and hardware test stages to pass the outcome. Learners can use partially pre-built circuits for hardware to save time. Learners should use contemporary debugging and hardware tools, including logic analysers. They should measure and evaluate timing characteristics during hardware testing.

Learners can produce a single report covering all the outcome's knowledge and skills requirements, and including critical self-reflection, as evidence. They should accompany this with demonstrations (these could be videos, screenshots or live) of working simulations and hardware.

Design, simulate, build, test and evaluate programmable logic device (PLD) circuits using a hardware description language (HDL) (outcome 3)

You should encourage learners to work together during formative assessment to fault-find and solve problems. You should provide HDL examples for formative assessment and learners should share their code with their peers.

For summative assessment, learners should edit library HDL examples to design a sequential FSM. Ideally, this should be the same FSM designed for summative assessment in outcome 2. Simulation testing should include static and dynamic (timing) parameters and make best use of debugging and evaluation IDE tools. At the synthesis stage, learners should optimise for at least one key characteristic, and demonstrate understanding of the requirements for optimisation for all the other characteristics listed in the knowledge requirements.

Learners can produce a single report covering all the outcome's knowledge and skills requirements, and including critical self-reflection, as evidence. They should accompany this with demonstrations (these could be videos, screenshots or live) of working simulations and synthesis.

Equality and inclusion

This unit is designed to be as fair and as accessible as possible with no unnecessary barriers to learning or assessment.

You should take into account the needs of individual learners when planning learning experiences, selecting assessment methods or considering alternative evidence.

Guidance on assessment arrangements for disabled learners and/or those with additional support needs is available on the assessment arrangements web page: www.sqa.org.uk/assessmentarrangements.

Information for learners

Digital Electronics: Digital System Design (SCQF level 8)

This information explains:

- what the unit is about
- what you should know or be able to do before you start
- what you need to do during the unit
- opportunities for further learning and employment

Unit information

This unit provides you with knowledge and skills specific to electronics engineering. It covers:

- characteristics and use of analogue to digital converters (ADCs)
- characteristics and use of digital to analogue converters (DACs)
- design and use of finite state machines (FSMs)
- programmable logic devices (PLDs) and hardware description language (HDL)

The unit is part of the Higher National Diploma (HND) in Engineering, which is aimed at learners who want to become engineering technicians in electronics, or control and instrumentation. The unit also provides you with knowledge and skills to go on to further study.

Before starting the unit, we recommend that you have knowledge and understanding of digital electronics. For example, you may have passed an SCQF level 7 (HNC level) qualification in a subject related to electronics principles.

Unit outcomes

On completion of the unit, you can:

1 design, simulate, build, test and evaluate analogue to digital converter (ADC) and digital to analogue converter (DAC) conversion circuits
2 design, simulate, build, test and evaluate sequential finite state machines (FSMs)
3 design, simulate, build, test and evaluate programmable logic device (PLD) circuits using a hardware description language (HDL)

In outcome 1, you learn about ADCs and DACs. You learn about their architectures, functions and specifications. Then you move on to design, simulate, build and test circuits that convert real-world analogue signals to computer-compatible digital signals, then back again to analogue signals.

In outcome 2, you learn about sequential FSMs, which perform a sequence of monitoring and control tasks. Building on your knowledge of combinational and sequential logic, you design, simulate, build and test sequential FSMs, and optimise them to best suit their application.

In outcome 3, you learn about contemporary programmable devices and HDL. You learn how to write, debug and simulate circuits written in HDL, using a modern integrated development environment (IDE). Building on the knowledge you gained in outcome 2, you design, simulate and synthesise digital circuits written in HDL.

You must generate evidence under unsupervised, open-book conditions.

You are assessed by completing mini projects, technical reports and critical self-evaluation. You collate your assessment evidence in a portfolio.

Meta-skills

Throughout the unit, you can develop meta-skills to enhance your employability in the engineering sector.

Meta-skills include self-management, social intelligence and innovation.

Self-management

You develop the meta-skill of initiative as you fault-find and solve problems with your designs.

Social intelligence

You develop the meta-skills of communicating and collaborating as you work with other learners on activities.

Innovation

You develop your creativity when you come up with designs that are optimised to meet specified requirements.

Administrative information

Published: October 2023 (version 1.0)

Superclass: VE

History of changes

Version	Description of change	Date

Note: please check SQA's website to ensure you are using the most up-to-date version of this document.