# Course report 2024

## National 5 Practical Electronics

This report provides information on candidates' performance. Teachers, lecturers and assessors may find it useful when preparing candidates for future assessment. The report is intended to be constructive and informative, and to promote better understanding. You should read the report with the published assessment documents and marking instructions.

We compiled the statistics in this report before we completed the 2024 appeals process.

# Grade boundary and statistical information

## Statistical information: update on courses

Number of resulted entries in 2023: 685

Number of resulted entries in 2024: 761

## Statistical information: performance of candidates

### Distribution of course awards including minimum mark to achieve each grade

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|---|---|---|---|---|---|---|---|---|
| **A** | Number of candidates | 253 | Percentage | 33.2 | Cumulative percentage | 33.2 | Minimum mark required | 70 |
| **B** | Number of candidates | 183 | Percentage | 24.0 | Cumulative percentage | 57.3 | Minimum mark required | 60 |
| **C** | Number of candidates | 134 | Percentage | 17.6 | Cumulative percentage | 74.9 | Minimum mark required | 50 |
| **D** | Number of candidates | 92 | Percentage | 12.1 | Cumulative percentage | 87.0 | Minimum mark required | 40 |
| **No award** | Number of candidates | 99 | Percentage | 13.0 | Cumulative percentage | 100 | Minimum mark required | N/A |

We have not applied rounding to these statistics.

You can read the general commentary on grade boundaries in the appendix.

In this report:

- ‘most’ means greater than 70%
- ‘many’ means 50% to 69%
- ‘some’ means 25% to 49%
- ‘a few’ means less than 25%

You can find statistical reports on the statistics and information page of our website.

# Section 1: comments on the assessment

## Question paper

The question paper was structured in a similar way to the specimen question paper and previous question papers, containing questions that sampled the areas of circuit design, simulation and construction in approximately equal proportions.

Feedback indicated that the question paper was fair both in terms of course coverage and in terms of overall level of challenge.

## Practical activity

Overall, the practical activity functioned as intended. A few verified centres did not apply the marking instructions to standard, however any deviations in marks were within tolerance.

All aspects of each available task provided sufficient opportunity for candidates to demonstrate different levels of performance from analysis and design, through to build and test and final reporting.

The marking instructions supported by the Understanding Standards materials allowed assessors to give appropriate credit to key levels of performance in all areas of design, build and test, as well as allowing assessors to differentiate between different levels of performance in all key areas of design, build and test.

# Section 2: comments on candidate performance

## Areas that candidates performed well in

### Question paper

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|---|---|
| Question 1(a) | Most candidates could name, identify or describe the function of selected components. |
| Question 1(b)(i) & (ii) | Most candidates were able to use the data sheet to determine the value and tolerance of the resistor from its colour bands. |
| Question 1(b)(iii) | Most candidates could determine the minimum and maximum value of the resistor. |
| Question 2 | Most candidates could state safety precautions that must be taken when using a soldering iron. |
| Question 4(a) | Most candidates could complete a truth table for an AND gate. |
| Question 4(b) | Most candidates could identify the ANSI symbol for a NOR gate. |
| Question 4(c) | Most candidates could score at least 2 marks of the 3 available in the completion of a truth table for a combination of three logic gates. Where a column was incorrect, most candidates benefited from the 'carry on' rule. |
| Question 5(a) | Most candidates scored 1 of the 2 available marks for stating two reasons for simulating a circuit before it is constructed, with only some gaining full marks. |
| Question 6 | Most candidates could complete a pre-power up checklist. |
| Question 7(b) | Most candidates were able to identify the correct symbol for direct current, as shown on the multimeter. |
| Question 8(a) | Most candidates could identify an analogue waveform from a CRO screen. |

### Practical activity

Regardless of the practical activity task chosen, candidates did well at certain stages and found other stages challenging. For example, in all tasks candidates found creating circuit layout diagrams, creating test plans and final circuit analysis challenging. The more practical, less reflective tasks such as circuit construction were carried out reasonably well by candidates.

Most candidates did well in circuit construction. The variations in marks were mainly due to the experience of assessors with these practical aspects, the quality of tools provided and the manual dexterity of candidates.

The practical activity accounts for 51 marks of the available 70. By the time candidates come to this component they should be suitably experienced in these elements. It is essential that candidates have access to a suitable range of properly maintained tools and equipment, and that they are given suitable guidance to achieve these tasks. It is also essential that assessors are confident with the practical areas of electronics and not just the theoretical aspects, as candidates will achieve most marks for the practical elements.

## Areas that candidates found demanding

### Question paper

| | |
|---|---|
| Question 3(b) | Many candidates substituted the resistance of R4, rather than the total circuit resistance, leading to incorrect substitution and incorrect final answer. This led to significant 'carry on' calculations in question 3(c). |
| Question 3(c) | Many candidates could not calculate the power dissipated and were unsure of the correct formula to use from the data sheet. |
| Question 5(b) | When asked to identify simulation errors in the flashing LED circuit, many responses lacked the clarity and precision required to be awarded full marks. Answers such as 'connection of 555 pins' and 'resistance of R1 and/or R2' were not errors. |
| Question 7(a) | Many candidates were able to identify the probe 1 error, but most were unable to identify the correct current setting on the multimeter. |
| Question 7(c) | Most candidates were unable to state the most appropriate scale to check the resistance value, with many candidates giving no response. |
| Question 8(c) | Many candidates found converting milliseconds to seconds challenging when calculating the frequency of the signal. |
| Question 9(a) | Many candidates appeared to find the concept of voltage division across series resistors difficult to understand and as such were unable to apply the correct values to the potential divider formula. However, many candidates gained at least 1 mark for selecting the correct formula from the data sheet. |
| Question 9(b) | Most candidates did not achieve any marks for this question because they did not appear to understand the concept of ratios. |
| Question 9(c) | Candidates found this to be a challenging question with many candidates providing no response. Of those who did, many struggled to provide an adequate description of how a voltage divider and comparator circuit operates, with responses often lacking the clarity and precision required to be awarded full marks. |
| Question 10 | Most candidates were able to achieve at least 3 marks in the production of a block diagram. Choosing the correct gates and the physical layout of a block diagram was poorly answered. |
| Question 11 | In comparison to previous years, most candidates attempted the 'circuit diagram' question. Of those who did, many candidates were able to gain some marks, however very few achieved full marks. Use of correct circuit symbols was poor, and the use of nodes was limited. |

Where candidates were asked to 'describe' or 'explain', answers were often too short or lacked sufficient detail or technical accuracy to gain marks.

A very small number of candidates appeared not to have prepared for, or did not appreciate, the depth of understanding and application of knowledge required for the question paper.

## Practical activity

The initial analysis of the given problem was more demanding and accounts for 7 marks. Candidates who analysed the given task correctly achieved the maximum 7 marks, whereas others were guided and marked accordingly to proceed with the rest of the assignment.

# Section 3: preparing candidates for future assessment

## Question paper

Candidates answering questions which require either restricted or extended responses should be wary of over-elaboration. Some candidates could identify errors in simulation circuits but could not express themselves with the required degree of clarity or precision to gain full marks. Centres should encourage correct scientific terminology and remember that units are required, unless stated otherwise in the question. Candidates need to be aware that the types of answers for circuit errors are very similar to pre-power up checklists for a circuit.

Candidates should pay attention to the command word used in each question and respond accordingly to gain marks.

Centres should ensure that candidates can describe, in a succinct and precise way, how to use the various testing instruments described in the course specification which can be found on the Practical Electronics subject page of SQA's website

In terms of applying relationships, candidates found calculating the reference voltage of a LM741 comparator very challenging and may need more practise in voltage division in general, as well as the concept of ratios in the context of voltage division.

Candidates need to be able to explain how a voltage divider, as well as a comparator circuit, works. Many candidates did not appear to fully understand the relationship between voltage and resistance in a series circuit. Candidates must be aware that when they are asked to draw circuit diagrams, they should ensure that there is a node on the end of the V+ and 0V lines. They must also remember to label every component on their diagram, even if it is incomplete.

Centres should be aware that most typical 'A type' questions are those which require the candidate to take information from one conceptual format and present it in another, for example, in block diagrams or when transferring a layout diagram to a circuit diagram (or vice versa). These are typically the final two questions in the paper. Further practise opportunities in these two areas will benefit candidates in the external and also the internal assessment components of the course.

Centres should be aware that the question paper, although worth only 30% of the overall marks for the course assessment, still requires sufficient preparation time throughout the academic year.

## Practical activity

Centres should give candidates access to a suitable range of properly maintained tools and equipment. Candidates will need to gain experience of using these tools and equipment as well as the simulation software. There are various websites that will assist assessors with the conventions used in the practical application of electronics such as circuit layout, test

points, labelling components, etc as well as giving practical advice on how to develop good soldering skills.

The more demanding tasks of design, testing and reporting are dependent upon assessors guiding candidates to determine the key inputs and outputs of each circuit process, and to include a range of circuit performance results from their simulation, which will assist them when testing the actual solution built to compare actual test results with the simulation test results and the given task specification

Good circuit simulation should also include a range of circuit performance results. This will assist candidates when testing the actual practical solution that they will build to compare actual test results with the simulation results. This will also assist candidates in achieving marks in the construction section by giving them a steer as to where to include test points in their circuits, which should also assist with the reporting section.

The final 12 marks can be demanding for candidates. They consist of 7 marks for testing the solution and 5 marks for reporting and evaluation. The key to gaining these marks is the candidate's ability to keep clear and accurate project logbooks detailing the main stages in the task, and the ability to evaluate their actual completed circuit test results against the simulation test results and the given task specification.

# Appendix: general commentary on grade boundaries

SQA's main aim when setting grade boundaries is to be fair to candidates across all subjects and levels and maintain comparable standards across the years, even as arrangements evolve and change.

For most National Courses, SQA aims to set examinations and other external assessments and create marking instructions that allow:

- a competent candidate to score a minimum of 50% of the available marks (the notional grade C boundary)
- a well-prepared, very competent candidate to score at least 70% of the available marks (the notional grade A boundary)

It is very challenging to get the standard on target every year, in every subject, at every level. Therefore, SQA holds a grade boundary meeting for each course to bring together all the information available (statistical and qualitative) and to make final decisions on grade boundaries based on this information. Members of SQA's Executive Management Team normally chair these meetings.

Principal assessors utilise their subject expertise to evaluate the performance of the assessment and propose suitable grade boundaries based on the full range of evidence. SQA can adjust the grade boundaries as a result of the discussion at these meetings. This allows the pass rate to be unaffected in circumstances where there is evidence that the question paper or other assessment has been more, or less, difficult than usual.

- The grade boundaries can be adjusted downwards if there is evidence that the question paper or other assessment has been more difficult than usual.
- The grade boundaries can be adjusted upwards if there is evidence that the question paper or other assessment has been less difficult than usual.
- Where levels of difficulty are comparable to previous years, similar grade boundaries are maintained.

Every year, we evaluate the performance of our assessments in a fair way, while ensuring standards are maintained so that our qualifications remain credible. To do this, we measure evidence of candidates' knowledge and skills against the national standard.

During the pandemic, we modified National Qualifications course assessments, for example we removed elements of coursework. We kept these modifications in place until the 2022–23 session. The education community agreed that retaining the modifications for longer than this could have a detrimental impact on learning and progression to the next stage of education, employment or training. After discussions with candidates, teachers, lecturers, parents, carers and others, we returned to full course assessment for the 2023–24 session.

SQA's approach to awarding was announced in March 2024 and explained that any impact on candidates completing coursework for the first time, as part of their SQA assessments, would be considered in our grading decisions and incorporated into our well-established

grading processes. This provides fairness and safeguards for candidates and helps to provide assurances across the wider education community as we return to established awarding.

Our approach to awarding is broadly aligned to other nations of the UK that have returned to normal grading arrangements.

For full details of the approach, please refer to the National Qualifications 2024 Awarding — Methodology Report.